## CLAIMS

1. A monotonous counter formed as an integrated circuit, each counting bit being provided by a memory cell (11, 11'; 11") containing at least one memorization element (Rp; Rp1, Rp2) formed of a polysilicon resistor, programmable by irreversible decrease in its value.

2. The counter of claim 1, wherein the programming of said resistor (Rp; Rp1, Rp2) is performed by temporarily submitting it to a constraint current greater than a current for which its value exhibits a maximum.

3. The counter of claim 1, comprising a circuit (30) for decoding the states contained in said cells (11, 11'; 11") for providing the resulting count.

4. The counter of claim 1, wherein each counting cell (11") comprises, in parallel between two terminals (12, 13) of application of a supply voltage (Vp, Vr), two branches each comprising:

a first polysilicon programming resistor (Rp1, Rp2) connected between a first supply terminal (12) and a terminal of differential reading (24, 26) of the cell state; and

at least one programming switch (MN1, MN2) connecting one of said read terminals to the second supply terminal (13).

5. The counter of claim 4, wherein each branch comprises a programming switch.

6. The counter of claim 4, wherein said programming resistors (Rp1, Rp2) are two polysilicon resistors identical in size and in possible doping.

7. The counter of claim 1, wherein each counting cell (11, 11') comprises a programming transistor (MN, MP) in series with a programming resistor (Rp).

8. The counter of claim 1, further comprising a circuit for controlling the programming of each of the counting cells (11, 11'; 11"), capable of providing individual control signals to the programming switches.